CLAIMS

What is claimed is:

1. A method of forming a semiconductor structure, comprising:

providing a nitride layer between a silicon-containing layer and a polysilicon layer.

2. The method of claim 1, further comprising:

forming an amorphous silicon layer, to provide said silicon-containing layer.

3. The method of claim 1, further comprising:

forming a polysilicon layer, to provide said silicon-containing layer.

4. The method of claim 1, further comprising:

forming a SiGe layer, to provide said silicon-containing layer.

5. The method of claim 1, wherein a grain size of said silicon-containing layer is smaller than that of said polysilicon layer.

6. The method of claim 1, wherein said silicon-containing layer is formed below said polysilicon layer.

7. The method of claim 1, wherein said nitride layer comprises a silicon nitride layer.

8. The method of claim 1, wherein said semiconductor structure comprises a gate stack.

9. The method of claim 1, wherein said nitride layer is formed on a surface of said silicon-containing layer and said polysilicon layer is formed on a surface of said nitride layer.

10. The method of claim 1, wherein said silicon-containing layer has a grain size substantially within a range of about 10 nm to about 20nm.

11. The method of claim 5, wherein said grain size of said silicon-containing layer is substantially within a range of about 10 nm to about 20nm.

12. The method of claim 1, further comprising:

depositing one of an amorphous Si, a polysilicon, and poly-SiGe as said silicon-containing layer.

13. The method of claim 12, wherein said one of the amorphous silicon, the polysilicon, and the poly-SiGe has a thickness of about 10 nm to about 20nm.

14. The method of claim 1, wherein said nitride layer has a thickness within a range of about 5 Å to about 15Å.

15. The method of claim 1, further comprising:

forming said silicon-containing layer on a gate dielectric,

said gate dielectric being formed on a substrate.

16. The method of claim 15, wherein said substrate comprises any of a bulk silicon substrate, a silicon-on-insulator, and a SiGe substrate.

17. The method of claim 15, wherein said gate dielectric has a thickness within a range of about 9 Å to about 50 Å.

18. The method of claim 15, wherein said gate dielectric comprises any of an oxide, an oxynitride, and an oxide-nitride stack combination.

19. The method of claim 2, wherein said amorphous Si is deposited at a temperature below 550 °C.

20. The method of claim 3, wherein said polysilicon is deposited at a temperature below 550 °C.

21. The method of claim 12, wherein said nitride layer is formed by a furnace anneal on said one of the amorphous silicon, the polysilicon, and the poly-SiGe.

22. The method of claim 21, wherein said nitride layer is formed by said furnace anneal at a temperature within a range of about 550 °C to about 750 °C.

23. The method of claim 21, wherein said nitride layer is formed by said furnace anneal in an ammonia ambient.

24. The method of claim 22, wherein said nitride layer is formed by said furnace anneal for about 5 minutes to about 20 minutes.

25. The method of claim 24, wherein said nitride layer is formed by said furnace anneal for about 15 minutes.

26. The method of claim 1, wherein said polysilicon layer has a thickness within a range of about 80nm to about 130 nm.

27. A method of making a semiconductor structure, comprising:

forming a gate stack including a silicon-containing layer and a polysilicon layer with a nitride layer therebetween,

wherein the silicon-containing layer sets the polysilicon grain size.

28. A method of forming a gate stack, comprising:

providing a nitride layer between a silicon-containing layer and a polysilicon layer,

wherein said silicon-containing layer has a grain size substantially within a range of about 10 nm to about 20nm.

29. A semiconductor structure, comprising:

a first polysilicon layer;

a second polysilicon layer formed over said polysilicon layer; and

a nitride layer formed between said first and second polysilicon layers,

wherein a grain size of said first polysilicon layer is smaller than that of said second polysilicon layer.

30. The structure of claim 29, wherein said first polysilicon layer has a grain size substantially within a range of about 10 nm to about 20nm.

31. The structure of claim 29, wherein said nitride layer has a thickness within a range of about 5 Å to about 15Å.

32. The structure of claim 29, further comprising:

a gate dielectric on which said first polysilicon layer is formed; and

a substrate on which said gate dielectric is formed.

33. The structure of claim 32, wherein said substrate comprises any of a bulk silicon substrate, a silicon-on-insulator, and a SiGe substrate.

34. The structure of claim 32, wherein said gate dielectric has a thickness within a range of about 9 Å to about 50 Å.

35. The structure of claim 32, wherein said gate dielectric comprises any of an oxide, an oxynitride, and an oxide-nitride stack combination.

36. The apparatus of claim 29, wherein said second polysilicon layer has a thickness within a range of about 80nm to about 130 nm.

37. A gate stack, comprising:

a first polysilicon layer;

a second polysilicon layer; and

a nitride layer formed between said first and second polysilicon layers,

wherein said first polysilicon layer has a grain size substantially within a range of about 10 nm to about 20nm.